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PRE-APPEAL BRIEF REQUEST FOR REVIEW		Docket Number (Optional) SC11370TH	
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]		Application Number 10/054,577	Filed November 13, 2001
on <u>12-20-05</u>		First Named Inventor	
Signature <u>Pat Thomas</u>		William C. Moyer	
Typed or printed name <u>Pat Thomas</u>		Art Unit 2183	Examiner Tonia L. Meonske
Applicant request review of the final rejection in the above identified application. No amendments are being filed with this request.			
This request is being filed with a notice of appeal.			
The review is requested for the reason(s) stated on the attached sheet(s). Note: No more than five (5) pages may be provided.			
I am the			
<input type="checkbox"/> applicant/inventor.		Signature	
<input type="checkbox"/> assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)		<u>Joanna G. Chiu</u> Typed or printed name	
<input checked="" type="checkbox"/> attorney or agent of record. Registration number <u>43,629</u>		<u>(512) 996-6839</u> Telephone number	
<input type="checkbox"/> attorney or agent acting under 37 CFR 1.34 Registration number if acting under 37 CFR 1.34 _____		_____	
NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.			
<input checked="" type="checkbox"/> *Total of <u>1</u> forms are submitted			

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UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S) William C. Moyer et al. GROUP ART UNIT: 2183
APPLN. NO.: 10/054,577 EXAMINER: Tonia L. Moenske
FILED: November 13, 2001
TITLE: METHOD AND APPARATUS FOR INTERFACING A PROCESSOR
TO A COPROCESSOR IN WHICH THE PROCESSOR IS CAPABLE
OF SELECTIVELY BROADCASTING TO OR SELECTIVELY
ALTERING AN EXECUTION MODE OF THE COPROCESSOR

STATEMENT OF REASONS FOR PRE-APPEAL BRIEF REVIEW

Applicant respectfully requests review of the Final Rejection mailed September 22, 2005. In the current Application, claims 1-5, 9, 10, and 13-20 are currently pending. In the Final Rejection, claims 1-5 and 9 are rejected under 35 U.S.C. 102(b) over US Patent 6,047,122 (hereinafter referred to as Spiller), and claims 10 and 13-20 are rejected under 35 U.S.C. 103 over US Patent 6,138,185 (hereinafter referred to as Nelson).

Rejection of Claims 1-5 and 9

Applicant submits that claims 1-5 and 9 are patentable over Spiller because Spiller does not teach or suggest each and every element of the claims. For example, with respect to claims 1 and 9, the Examiner states that the processor of claims 1 and 9 is taught by processor 200 of Spiller which the Examiner contends has a register file. The Examiner further states that elements 855, 860, and 863 "also comprise the register file." However, note that elements 855, 860, and 863 (described in reference to FIG. 7B-2A) are located within control network interface 204 (see FIGs. 6 and 7B), and more specifically, located in registers 804 (see FIG. 7B, col. 45, lines 28-30, and col. 45, line 55 - col. 46, lines 2, where FIG. 7B is a general block diagram of control network interface 204). Therefore, Applicant firstly submits that elements 855, 860, and 863 are not a part of processor 200's register file. They are located outside processor 200 in network interface 202. The Examiner relies on operands being provided to elements 855, 860, and 863 to anticipate claim 1; however, these elements are not part of processor 200's register file. Therefore, Spiller does not teach or suggest providing to the register file of processor 200 said operand to be written to said register file and selectively

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providing via said coprocessor communication bus said operand to be written in said register file, as claimed in claims 1 and 9.

Therefore, for at least these reasons, Applicant submits that claims 1 and 9 are patentable over Spiller.

Furthermore, even if the Examiner is correct in assuming that elements 855, 860, and 863 may be considered part of processor 200's register file (which Applicant does not concede), the operands from 855, 860, and 863 are not being provided to said register file *and* selectively provided via said coprocessor communication bus, as claimed in claims 1 and 9. That is, if the Examiner considers the registers of processor 200 and elements 855, 860, and 863 to be "the register file", then the elements are only being provided *from the register file of Spiller to the register file of Spiller*. According to the Examiner's analysis, the operands of elements 855, 860, and 863 are only provided from the register file of processor 200 (i.e. elements 855, 860, and 863) to the register file of processor 200 (the registers in processor 200). Therefore, the operands stored in elements 855, 860, and 863 are never being selectively provided "via said coprocessor communication bus." A coprocessor communication bus communicates with a coprocessor, and the values stored in elements 855, 860, and 863 are never provided to a coprocessor or to a coprocessor communication bus. Furthermore, Spiller does not even teach or suggest a coprocessor communication bus which is coupled to processor 200, and thus cannot teach or suggest selectively providing operands via a coprocessor communication bus. Therefore, for at least these additional reasons, Applicant submits that claims 1 and 9 are patentable over Spiller.

With respect to claim 1, the Examiner states that elements 850, 851, and 852 teach the broadcast specifiers. However, Spiller does not teach or suggest selectively providing via said coprocessor communication bus said operand to be written in said register file based on the elements 850, 851, and 852. For example, the Examiner states that elements 850, 851, and 852 enable an operand to be provided *to the register file of the processor, through a coprocessor communication bus, by asserting a POP signal*. Firstly, the operands from elements 855, 860, and 863 are not provided via a coprocessor communication bus. By the Examiner's own admission, the operands are provided to the register file *of the processor* where the communication occurs over memory bus 203 which is not a bus which communicates with a coprocessor. Secondly, elements 850, 851, and 852 are simply registers and do not assert the POP signal. That is, the POP signal is not generated based on these registers. The POP signal of Spiller is asserted by

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circuitry in network interface 202, but there is no teaching or suggestion of the registers themselves asserting this signal, or of using these registers in any way to generate the POP signal. Therefore, for at least these additional reasons, Applicant submits that claim 1 is patentable over Spiller.

With respect to claim 9, Spiller also does not teach or suggest "selectively providing via said coprocessor bus said operand to be written in said register file based on a current execution region of said processor." The Examiner states that "the current execution region of said processor" is taught by elements 833-835, which are indicated by "SBC", "BC", and "COM", respectively. However, elements 833-835 (the receive FIFOs) have nothing to do with execution regions of processor 200. Furthermore, elements 833-835 are simply storage elements and are not related to execution at all. Also, as already discussed above, elements 850, 851, and 852 do not teach or suggest the broadcast specifier; they are simply registers and do not assert the POP signal. That is, the POP signal is not generated based on these registers. The POP signal of Spiller is asserted by circuitry in interface 202, but there is no teaching or suggestion of the registers themselves asserting this signal, or of using these registers in any way to generate the POP signal. Furthermore, the POP signal of Spiller is generated independent of the current execution region of processor 200. Therefore, for at least these additional reasons, Applicant submits that claim 9 is patentable over Spiller.

Claims 2-5 depend directly or indirectly from allowable claim 1 and are therefore allowable for at least those reasons which apply to claim 1.

Rejections of Claims 10 and 13-20 under 35 U.S.C. 103(a)

Applicant submits that claims 10 and 13-20 are patentable over Nelson because Spiller does not teach or suggest each and every element of the claims. For example, claim 10 is directed to a processor comprising a plurality of registers. Claim 10 also includes a set of broadcast specifiers where each broadcast specifier comprises a set of broadcast indicators where each broadcast indicator corresponds to a register of the plurality of registers and indicates whether or not a write to the corresponding register is to be broadcasted. Claim 10 further includes compare circuitry for providing a broadcast enable signal where the broadcast enable signal enables broadcasting when the corresponding broadcast indicator indicates broadcasting for the one of the plurality of registers and the broadcast signal does not enable broadcasting when the corresponding broadcast indicator does not indicate broadcasting for the one of the plurality of registers. Therefore, note that, in claim 10, the broadcast specifiers, broadcast indicators, compare

circuitry, and broadcast enable signal all interact in some way with the plurality of registers of the processor. Nelson only mentions that the crossbar switch interconnects data for point-to-point communications between servers, storage systems, workstations, switches, and hubs, as cited by the Examiner. However, there is no description at all in Nelson as to any specifics of the processors themselves or of the registers in these processors.

The Examiner agrees that Nelson has not specifically taught a plurality of registers, but proceeds to state that Nelson has taught that the switch of Figure 2 interconnects data for point-to-point communications between servers, storage systems, workstations, switches, and hubs and that "using registers to store operand data is well known in storage systems and in processors in workstations for high speed access to the data." The Examiner then concludes that "it would have been obvious ... to have the storage of data in Nelson, be stored in registers, for the desirable purpose of high speed access to the data operands." However, claim 10 claims more than the mere existence of registers in which to store operands. As was described in the previous paragraph, claim 10 describes novel ways to associate such elements as broadcast specifiers, broadcast indicators, compare circuitry, and a broadcast enable signal with the plurality of registers, as well as describe some of their interactions. While Nelson does discuss "broadcast and multicast groups" in col. 8, this is in reference to the crossbar switch and has no specific relation to any registers within a processor coupled to the crossbar switch. Therefore, Applicant respectfully submits that the Examiner has failed to make a prima facie case of obviousness because Nelson clearly does not teach or suggest each and every element of claim 10. For at least these reasons, Applicant submits that claim 10 is allowable over Nelson.

With respect to claim 18, Applicant also submits that the Examiner has failed to make a prima facie case of obviousness because Nelson also does not teach or suggest each and every element of claim 18. Claim 18 is directed to a processor having a plurality of registers, a program counter unit, an execution region control unit, and a port including at least one coprocessor communication signal indicating a current execution region from the set of execution regions when the indicated address location falls within one of the set of execution regions. As stated previously with respect to claim 10, Nelson only mentions that the crossbar switch interconnects data for point-to-point communications between servers, storage systems, workstations, switches, and hubs, as cited by the Examiner. However, there is no description at all in Nelson as to any

specifics of the processors themselves or of the registers, program counter, or execution units in these processors.

Furthermore, the Examiner states that, in Nelson, "an address D0-D7 is indicated being between 0xF0 and 0xFF.)" However, this address is not an address indicated by the program counter of a particular processor nor is the range of 0xF0 and 0xFF indicative of an execution region of the particular processor. These addresses in Nelson are destination port addresses for the crossbar switch, and a port address of 0xF0 to 0xFF simply identifies a multicast or broadcast configuration of the crossbar switch but does not identify whether the program counter of a particular processor is within an execution region. That is, destination ports of the crossbar switch in Nelson may be "grouped" such that the ports in the group can be concurrently connected to a single requesting source port (see col. 8, lines 52-55). However, these groupings are independent of the program counter of a processor. Furthermore, there is no signal indicating a current execution region from a set of execution regions of a processor. Therefore, for at least these reasons, Applicant submits that claim 18 is allowable over Nelson.

Claims 13-17 and 19-20 depend directly or indirectly from allowable claims 10 or 18 and are therefore allowable for at least those reasons provided with respect to claims 10 and 18.

Conclusion

Applicant respectfully solicits allowance of the pending claims. Contact me if there are any issues regarding this communication or the current Application.

If Applicant has overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 503079, Freescale Semiconductor, Inc.

Respectfully submitted,

SEND CORRESPONDENCE TO:

Freescale Semiconductor, Inc.
Law Department

Customer Number: 23125

By: 

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FEE TRANSMITTAL Patent fees are subject to annual revision <input type="checkbox"/> Applicant claims small entity status. See 37 CFR 1.27		<i>Complete if Known</i>		
		Application Number	10/054,577	RECEIVED CENTRAL FAX CENTER
		Filing Date	November 13, 2001	DEC 20 2005
		First Named Inventor	William C. Moyer	
		Examiner Name	Tonia L. Meonske	
		Group Art Unit	2183	
TOTAL AMOUNT OF PAYMENT		(\$ 500)	Attorney Docket No. SC11370TH	

METHOD OF PAYMENT (check all that apply) <input type="checkbox"/> Check <input type="checkbox"/> Credit card <input type="checkbox"/> Money Order <input type="checkbox"/> Other <input type="checkbox"/> None <input checked="" type="checkbox"/> Deposit Account: Deposit Account Number <u>503079</u> Deposit Account Name <u>FREESCALE SEMICONDUCTOR, INC.</u> The Director is authorized to: (check all that apply) <input checked="" type="checkbox"/> Charge fee(s) indicated below <input checked="" type="checkbox"/> Credit any overpayments <input checked="" type="checkbox"/> Charge any additional fee(s) during the pendency of this application <input type="checkbox"/> Charge fees(s) indicated below, except for the filing fee to the above-identified deposit account.	FEE CALCULATION (continued) 3. ADDITIONAL FEES <table style="width:100%; border-collapse: collapse;"> <thead> <tr> <th colspan="2">Large Entity</th> <th colspan="2">Small Entity</th> <th rowspan="2">Fee Description</th> </tr> <tr> <th>Fee Code</th> <th>Fee (\$)</th> <th>Fee Code</th> <th>Fee (\$)</th> </tr> </thead> <tbody> <tr><td>1051</td><td>130</td><td>2051</td><td>65</td><td>Surcharge - late filing fee or oath</td></tr> <tr><td>1052</td><td>50</td><td>2052</td><td>25</td><td>Surcharge - late Provisional filing</td></tr> <tr><td>1053</td><td>130</td><td>1053</td><td>130</td><td>Non-English specification</td></tr> <tr><td>1812</td><td>2520</td><td>1812</td><td>2520</td><td>For filing a request for ex parte Reexamination</td></tr> <tr><td>1804</td><td>920*</td><td>1804</td><td>920*</td><td>Requesting publication of SIR prior to Examiner action</td></tr> <tr><td>1805</td><td>1840*</td><td>1805</td><td>1840*</td><td>Requesting publication of SIR after Examiner action</td></tr> <tr><td>1251</td><td>120</td><td>2251</td><td>60</td><td>Extension for reply within first month</td></tr> <tr><td>1252</td><td>450</td><td>2252</td><td>225</td><td>Extension for reply within second month</td></tr> <tr><td>1253</td><td>1020</td><td>2253</td><td>510</td><td>Extension for reply within third month</td></tr> <tr><td>1254</td><td>1590</td><td>2254</td><td>795</td><td>Extension for reply within fourth month</td></tr> <tr><td>1255</td><td>2160</td><td>2255</td><td>1080</td><td>Extension for reply within fifth month</td></tr> <tr><td>1401</td><td>500</td><td>2401</td><td>250</td><td>Notice of Appeal</td></tr> <tr><td>1402</td><td>500</td><td>2402</td><td>250</td><td>Filing a brief in support of an appeal</td></tr> <tr><td>1403</td><td>1000</td><td>2403</td><td>500</td><td>Request for oral hearing</td></tr> <tr><td>1451</td><td>1510</td><td>1451</td><td>1510</td><td>Petition to Institute a public use proceeding</td></tr> <tr><td>1452</td><td>110</td><td>2452</td><td>55</td><td>Petition to revive - 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SUBMITTED BY Name (Print/Type) <u>Joanna G. Chiu</u> Signature		Complete (if applicable) Registration No. <u>43,629</u> Telephone <u>(512) 996-6839</u> Date <u>12/20/05</u>	
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FEE TRANSMITTAL Patent fees are subject to annual revision <input type="checkbox"/> Applicant claims small entity status. See 37 CFR 1.27		<i>Complete if Known</i>		
		Application Number	10/054,577	
		Filing Date	November 13, 2001	
		First Named Inventor	William C. Moyer	
		Examiner Name	Tonia L. Meonske	
TOTAL AMOUNT OF PAYMENT		(\$ 500)	Attorney Docket No.	SC11370TH

METHOD OF PAYMENT (check all that apply)

☐ Check
 ☐ Credit card
 ☐ Money Order
 ☐ Other
 ☐ None

☒ Deposit Account:

Deposit Account Number: **503079**
 Deposit Account Name: **FREESCALE SEMICONDUCTOR, INC.**

The Director is authorized to: (check all that apply)

☒ Charge fee(s) indicated below
 ☒ Credit any overpayments

☒ Charge any additional fee(s) during the pendency of this application

☐ Charge fees(s) indicated below, except for the filing fee to the above-identified deposit account.

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity		Small Entity		Fee Description
Fee Code	Fee (\$)	Fee Code	Fee (\$)	
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SUBTOTAL (1)		(\$)		

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2. EXTRA CLAIM FEES

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Multiple Dependent			200	
				360 =

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SUBTOTAL (2)		(\$)		

** or number previously paid, if greater; For Reissues, see above.

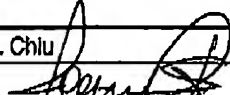
SUBTOTAL (3)

SUBTOTAL (3) (\$ 500)

* Reduced by Basic Filing Fee Paid

SUBMITTED BY

Name (Print/Type): **Joanna G. Chiu**

Signature: 

Complete (if applicable)

Registration No. **43,629** Telephone **(512) 996-6839**

Date **12/20/05**

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Austin, TX 78729

Telephone: (512) 996-6839
Facsimile: (512) 996-6854

11 Number of Pages (including this page)

Date: December 20, 2005
To: MS: AF, Examiner Tonia L. Meonske, Group Art Unit 2183
Location: United States Patent and Trademark Office
Fax No.: (571) 273-8300
From: Joanna G. Chiu, Registration No. 43,629
Subject: 10/054,577- William C. Moyer (Docket No. SC11370TH)

MESSAGE:

Enclosed herewith is a Notice of Appeal for the above-referenced patent application.

ALL ITEMS MARKED WITH AN "X" ARE INCLUDED IN THE FAX

1.	X	1 page Fax cover sheet
2.	X	1 page Notice of Appeal (in duplicate)
3.	X	1 page Pre-Appeal Request for Review
4.	X	5 page Statement of Reasons for Pre-Appeal Brief Review
5.	X	1 page Fee Transmittal (in duplicate)

Fee(s) charged to Deposit Account 503079, Freescale Semiconductor, Inc. \$500

Certificate of Transmission under 37 CFR 1.8

I hereby certify that this correspondence is being facsimile transmitted to the Patent and Trademark Office.

On 12-20-05

Signature

Pat Thomas
Printed Name of Person Signing Certificate

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